

Desicription

- ◆ ESD0303LR uses ultra-small DFN2.5*1.0-10L package. Each ESD0303LR device can protect four high-speed data lines. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make ESD0303LR ideal for high-speed data ports and high-frequency lines (e.g., USB3.0 & DVI) applications. The low clamping voltage of the ESD0303LR guarantees a minimum stress on the protected IC.

Features

- ◆ IEC61000-4-2(ESD): $\pm 15\text{KV}$ Max Air
 $\pm 15\text{KV}$ Max Contact
- ◆ IEC61000-4-4(EFT): $40\text{A}(5/50\text{ns})$
- ◆ IEC61000-4-5(Surge): $7.0\text{A}(8/20\mu\text{s})$
- ◆ Line capacitance: $0.25\text{pF}(\text{typical})@1\text{MHz}$
- ◆ Very low reverse current: $I_R < 0.1\mu\text{A}(\text{typical})$
- ◆ Halogen free ,Lead free and RoHs
- ◆ $70.0\text{ Watts Peak Pulse Power per Line}(t_p=8/20\mu\text{s})$

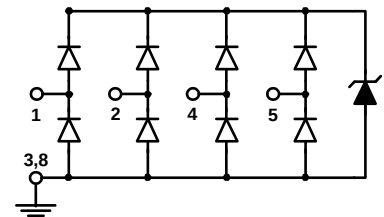
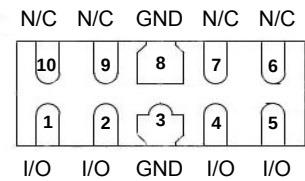
Application

- ◆ USB2.0&3.0
- ◆ V-By-One
- ◆ SATA and eSATA interface
- ◆ HDMI 1.3, 1.4,2.0 and 2.1
- ◆ PCI Express
- ◆ Desktops, Servers and Notebooks
- ◆ MDDI Ports
- ◆ 10G Ethernet Ports

Order information

Model	Marking	Package	shipping
ESD0303LR	a4	DFN2510-10L	3000/Tape&Reel

DFN-2510



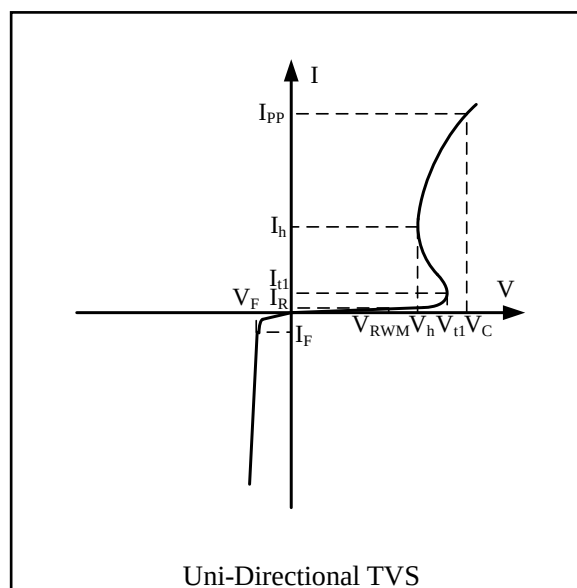
Circuit Diagram

Electrical characteristics (TA=25 °C, unless otherwise noted)

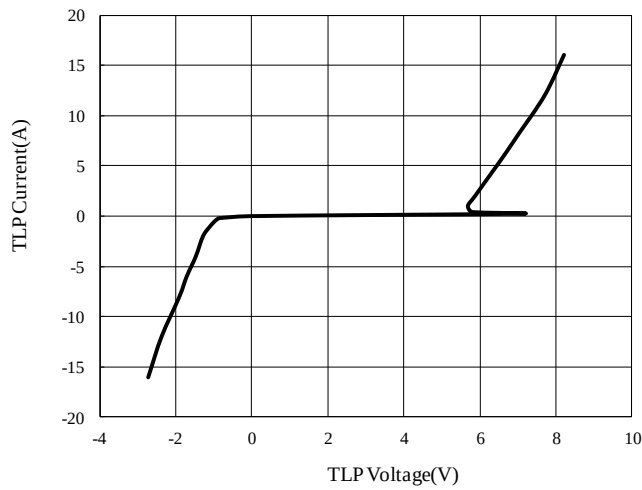
Parameter	Symbol	Conditions	Min.	TYP.	Max.	Units
Reverse stand-off voltage	V_{RWM}				3.3	V
Reverse leakage current	I_R I/O to GND	$V_{RWM}=3.3V$			0.1	uA
Reveres breakdown voltage	V_{BR} I/O to GND	$I_T=1mA$	5.0		9.0	V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	$t_p=10/100ns$		0.18		Ω
ESD Clamping Voltage	V_{clamp}	$I_{PP}=16A, t_p=10/100ns$		8.5		V
Clamping voltage	V_C I/O to GND	$I_{pp}= 7.0A (8/20us)$		9.0	11.0	V
Junction capacitance	C_J I/O to GND	$VR=1.65V f=1MHz$		0.25	0.35	pF

Electrical Characteristics (TA = 25°C)

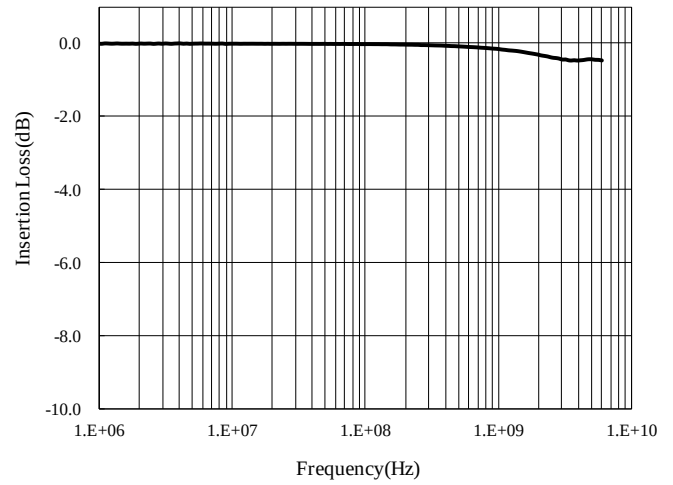
Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{t1}	Reverse Triggering Voltage @ I_{t1}
I_{t1}	Test Current for Reverse Triggering
V_h	Holding Voltage
I_h	Holding Current
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Peak Pulse Current
C_{ESD}	Parasitic Capacitance
f	Small Signal Frequency
V_F	Forward Voltage
I_F	Forward Current



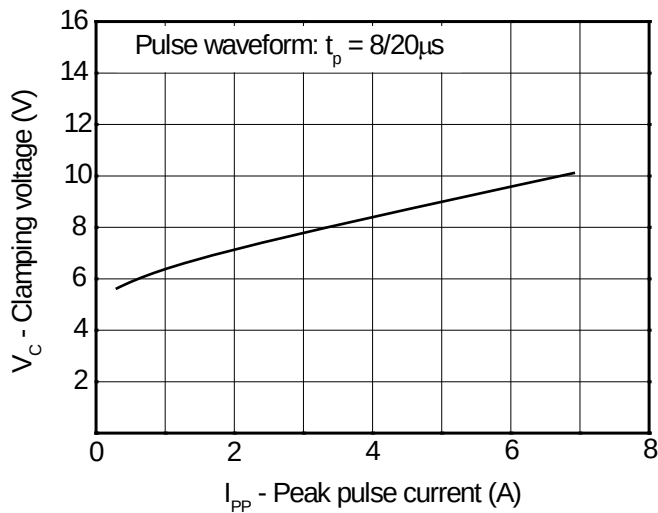
Typical characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)



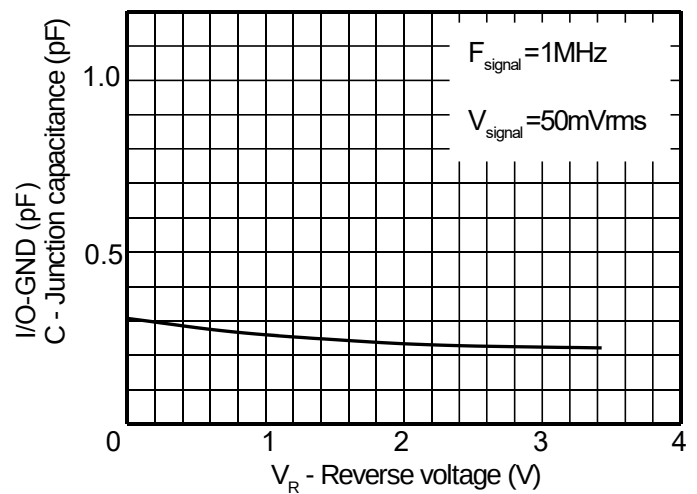
TLP Testing of I/O to GND



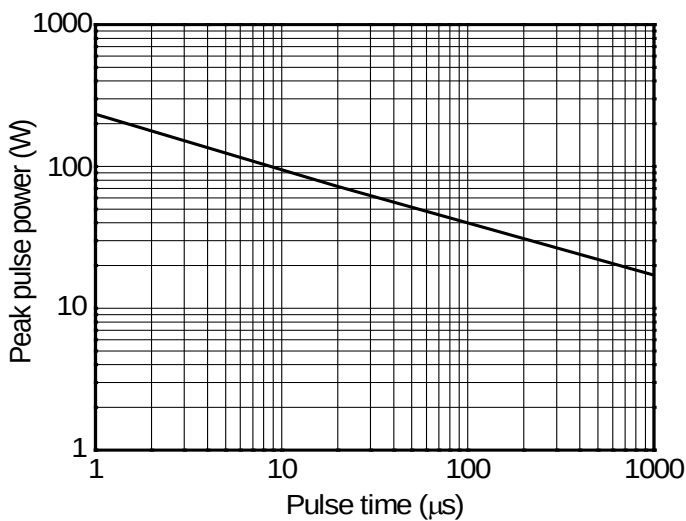
Insertion Loss S21 of I/O to GND



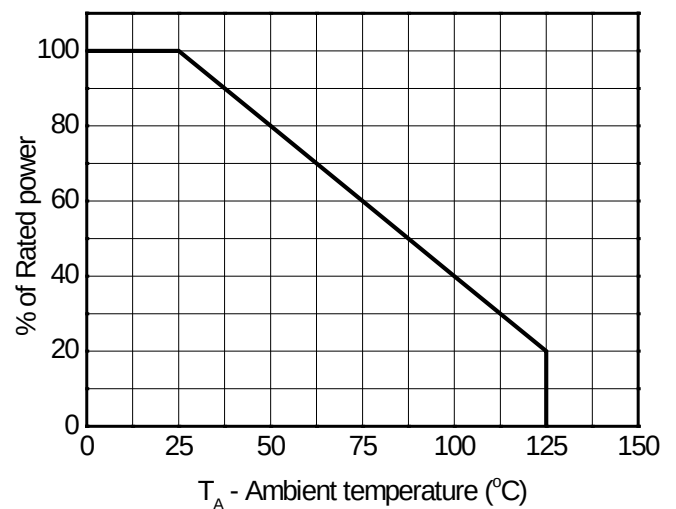
Clamping voltage vs. Peak pulse current



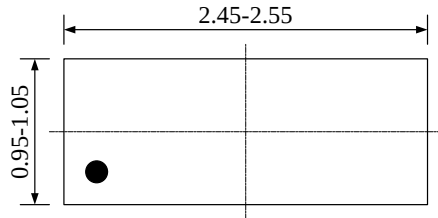
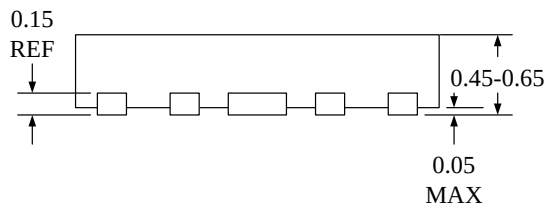
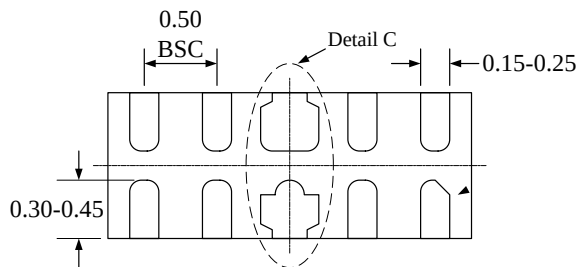
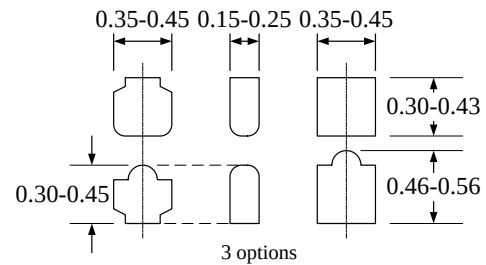
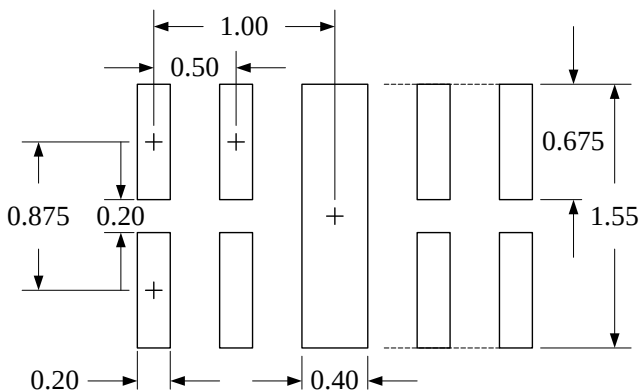
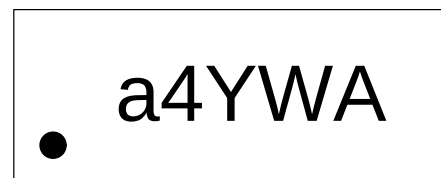
Capacitance vs. Reverse voltage



Non-repetitive peak pulse power vs. Pulse time



Power derating vs. Ambient temperature

Package outline dimensions
DFN2510-10L

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Detail C
PCB Layout Pattern

Marking Codes

Note

- (1) "a4" is device code, fixed,
- (2) "YWA" is date code.